Low offset, rail-to-rail output, 36V operational amplifier.

Description

SL2177F (dual) and SL4177F (quad) are low-offset operational amplifiers featuring high input impedance and output swing capability within 200mV of the supply rails. Their input common-mode voltage range extends to the negative supply rail. They utilize Trim technology for offset voltage calibration, resulting in exceptionally low offset voltage (typical value of 50μV).

The chip supports both single-supply and dual-supply configurations. In single-supply mode, the supply voltage range is from +3.3V to +36V. In dual-supply mode, the supply voltage range is from ±1.65V to ±18V.

The SL2177F is available in SOP-8 and MSOP-8 packages, while the SL4177F is offered in SOP-14 and TSSOP-14 packages. All package types have an operating temperature range of -40° C to +125° C.

Features

- Low offset voltage: 50μV (typical)
- Zero drift: 0.5μV/℃
- High DC precision
  - Open-loop gain (A_{VOL}): 120dB
  - Power supply rejection ratio (PSRR): 110dB
  - Common-mode rejection ratio (CMRR): 110dB
- Gain bandwidth product: 2MHz
- Static current: 400μA (typical)
- Power supply voltage range: ±1.65V to ±18V
- Rail-to-rail output
- Input extends to the negative supply rail

Applications

- Bridge amplifiers
- Strain gauges
- Sensor applications
- Temperature measurement
- Electronic scales
- Medical devices
- Resistance thermometers

Pin distribution

SL2177F
MSOP8/SOP-8

SL4177F
TSSOP-14/SOP-14

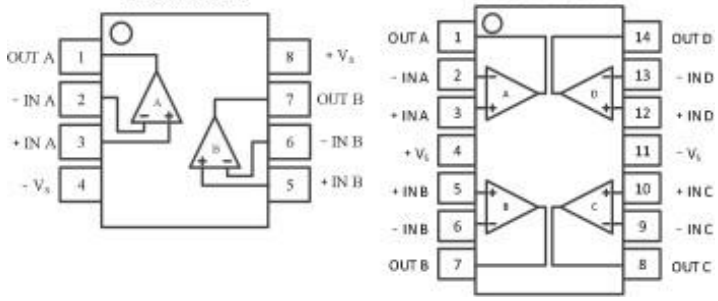


Fig.1 Pin Distribution

Pin description

Symbol	Description
+INA, +INB +INC, +IND	the non-inverting input of the operational amplifier
-INA, -INB -INC, -IND	the inverting input of the operational amplifier
$+V_S$	positive power supply terminal
$-V_S$	negative power supply terminal (connected to ground when single power supply is used)
OUTA, OUTB OUTC, OUTD	the output of the operational amplifier

Ordering information

Type	Package	Packing Quantity
SL2177FXS8	SOP-8	4000PCS
SL2177FXV8	MSOP-8	3000PCS
SL4177FXS14	SOP-14	2500PCS
SL4177FXT14	TSSOP-14	3000PCS

Absolute maximum ratings (T_A=25°C)

Symbol	Parameter	Rated Value	Unit
V_S	power supply voltage	±19，38（single power supply）	V
V_{CM}	common-mode voltage	V_{S-}-0.3 to V_{S+}+0.3	V
I_{IN}	input current	±10	mA
V_{DM}	differential voltage	±0.7	V
T_A	operating temperature	-40 to +125	℃
T_{STG}	storage temperature	-65 to +150	℃
T_J	junction temperature	150	℃
ESD	human body model (HBM)	2	kV

Remarks:

1.Exceeding the absolute maximum ratings may cause permanent damage to the device. The parameters listed above are only some critical ones, and exceeding normal operating ranges for other unlisted parameters should not be assumed. Prolonged operation at absolute maximum ratings may affect device reliability.

2. The input terminals are clamped to the power supply rails by diodes.

3. The device must never exceed the maximum junction temperature at any time.

Electrical parameters (T_A=25℃)

(V_S = ±18 V, T_A = 25°C, V_{CM} = V_S/2, V_O = V_S/2, R_L = 10 kΩ connected to V_S/2, unless otherwise noted.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input Characteristics						
V_{OS}	input offset voltage		-150	±50	150	μV
V_{OS} TC	offset voltage drift	T_A=-40℃ to +125℃		0.5		μV/℃
I_B	input bias voltage	V_{CM}=V_S/2		±100		pA
I_{OS}	input offset current			±100		pA
V_{CM}	common-mode input voltage range	T_A= -40℃ to +125℃	V_{S-}		(V_{S+}) -1.5	V
CMRR	common-mode rejection ratio open-loop voltage gain	V_{S-}<V_{CM}<V_{S+} -1.5V		110		dB
		T_A=-40℃ to +125℃		100		dB
A_{VOL}	input offset voltage	V_{S-}+0.5V<V_O<V_{S+}-0.5V		120		dB
		T_A=-40℃ to +125℃		110		dB
Output Characteristics						
V_{OH}	high output voltage swing	R_L= 10kΩ	(V_{S+}) -200	(V_{S+}) -120		mV
		T_A=-40℃ to +125℃	(V_{S+}) -280			mV
V_{OL}	low output voltage swing	RL=10kΩ		(V_{S-}) +110	(V_{S-}) +200	mV
		T_A=-40℃ to +125℃			(V_{S-}) +280	mV
I_{SC}	short-circuit output current	source current		25		mA
		sink current		25		mA
Power Characteristics						
PSRR	power supply rejection ratio	V_S=4V to 36V		110		dB
		T_A=-40℃ to +125℃		100		dB
I_Q	quiescent current (single channel)			410	550	μA
		T_A=-40℃ to +125℃			650	μA
Noise						
V_n	input voltage noise	f=0.1Hz to 10Hz		8		μVpp
e_n	input voltage noise density	f= 1kHz		22		nV/√Hz
Dynamic Characteristics						
GBW	gain bandwidth product	G=-10		2		MHz
SR	slew rate	G=+1		1.6		V/μs

Electrical parameters (T_A=25℃)

(V_S=±2.5V, T_A=25℃, V_{CM}=V_S/2, V_O=V_S/2, R_L=10kΩ connected to V_S/2, unless otherwise specified.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input Characteristics						
V_{OS}	input offset voltage		-150	±50	150	μV
V_{OS} TC	offset voltage drift	T_A=-40℃ to +125℃		0.5		μV/℃
I_B	input bias voltage	V_{CM}=V_S/2		±50		pA
I_{OS}	input offset current			±50		pA
V_{CM}	common-mode input voltage range	T_A= -40℃ to +125℃	V_{S-}		(V_{S+})-1.5	V
CMRR	common-mode rejection ratio open-loop voltage gain	V_{S-}<V_{CM}<V_{S+} -1.5V		95		dB
		T_A=-40℃ to +125℃		90		dB
A_{VOL}	input offset voltage	V_{S-}+0.5V<V_O<V_{S+}-0.5V		115		dB
		T_A=-40℃ to +125℃		105		dB
Output Characteristics						
V_{OH}	high output voltage swing	R_L= 10kΩ	(V_{S+})-30	(V_{S+})-20		mV
		T_A=-40℃ to +125℃	(V_{S+})-40			mV
V_{OL}	low output voltage swing	RL=10kΩ		(V_{S-})+20	(V_{S-}) +30	mV
		T_A=-40℃ to +125℃			(V_{S-}) +40	mV
I_{SC}	short-circuit output current	source current		25		mA
		sink current		25		mA
Power Characteristics						
PSRR	power supply rejection ratio	V_S=4V to 36V		110		dB
		T_A=-40℃ to +125℃		100		dB
I_Q	quiescent current (single channel)			390	540	μA
		T_A=-40℃ to +125℃			640	μA
Noise						
V_n	input voltage noise	f=0.1Hz to 10Hz		8		μV_{pp}
e_n	input voltage noise density	f= 1kHz		22		nV/√Hz
Dynamic Characteristics						
GBW	gain bandwidth product	G=-10		2		MHz
SR	slew rate	G=+1		1.5		V/μs

Typical performance characteristics

(V_S = ±18 V, T_A = 25°C, V_{CM} = VS/2, V_O = VS/2, R_L = 10 kΩ connected to V_S/2, unless otherwise noted.)

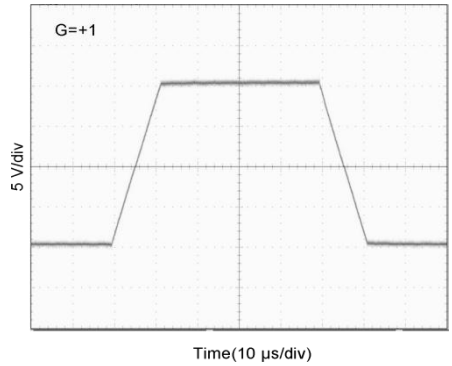


Fig.2 Large Signal Step Response

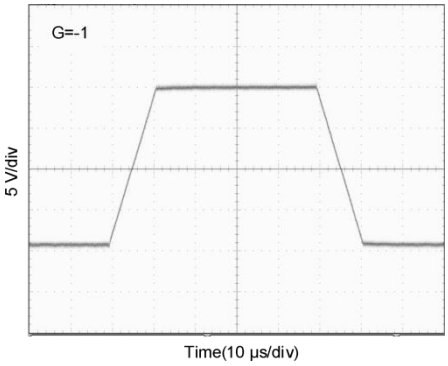


Fig.3 Large Signal Step Response

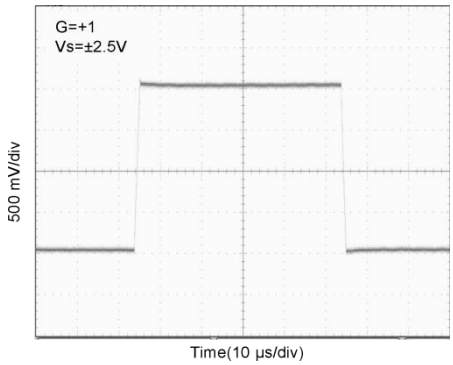


Fig.4 Large Signal Step Response

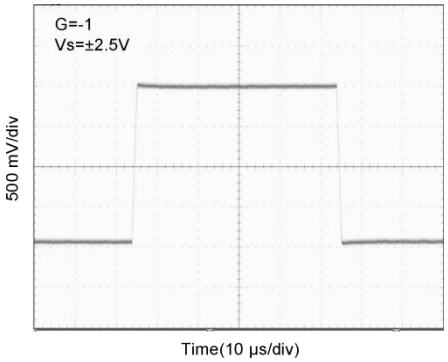


Fig.5 Large Signal Step Response

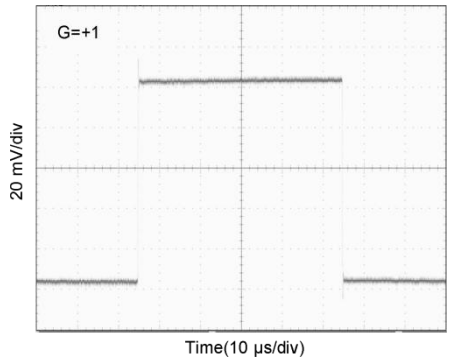


Fig.6 Small Signal Step Response

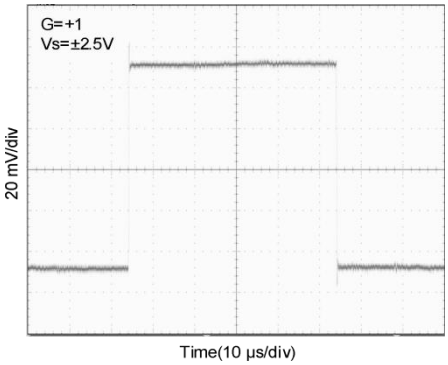


Fig.7 Small Signal Step Respons

Typical performance characteristics

(V_S = ±18 V, T_A = 25° C, V_{CM} = V_S/2, V_O = V_S/2, R_L = 10 kΩ connected to V_S/2, unless otherwise noted.)

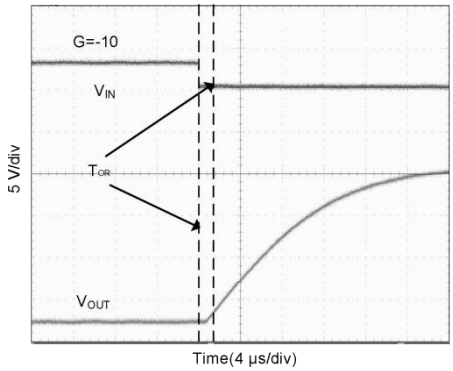


Fig.8 Negative Overload Recovery

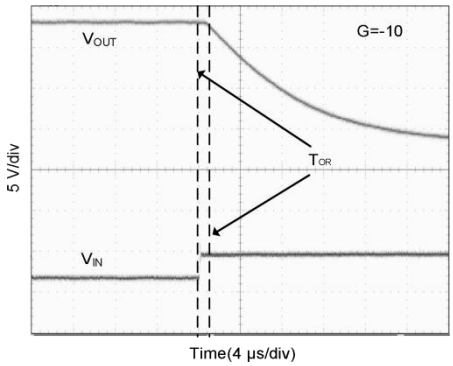


Fig.9 Positive Overload Recovery

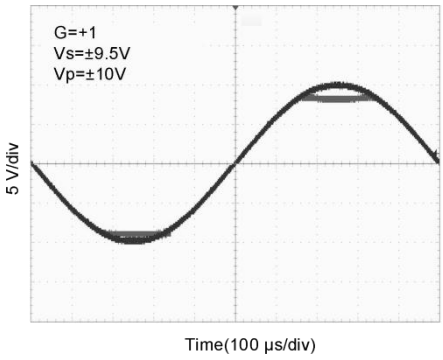


Fig.10 No Phase Flip

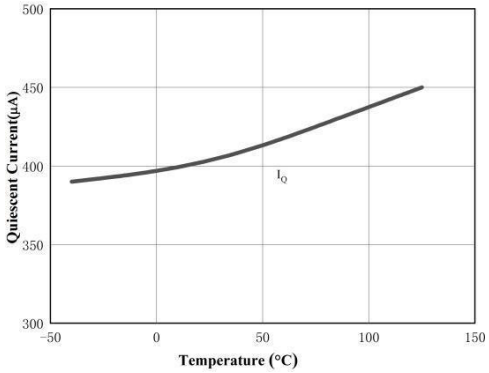


Fig.11 Quiescent Current vs. Temperatur

Application guide

1. Application information

The SL2177F and SL4177F series are low-offset operational amplifiers renowned for their exceptional performance, making them an ideal choice for many high-precision applications. They exhibit a drift of 0.5μV/℃ across the entire operating temperature range. Additionally, these amplifiers feature high CMRR, PSRR, and open-loop gain characteristics. In scenarios with high noise or high power supply impedance, decoupling capacitors (such as 0.1μF) should be placed adjacent to the power supply pins of the op-amp and positioned as close as possible to these pins.

2. Working characteristics

The specified supply voltage range for the SL2177F and SL4177F series is from 3.3V to 36V (±1.65V to ±18V). The operational temperature range is specified as -40° C to +125° C. Parameters related to supply voltage and temperature are typically tested under typical performance conditions.

3. Phase reversal protection

The SL2177F and SL4177F series feature phase reversal protection. In typical operational amplifiers, when the input voltage exceeds the common-mode input voltage range, the output phase can flip. This often occurs in non-inverting circuit configurations where the input voltage exceeds the specified common-mode voltage range, causing the output to flip and reach the supply rails. The SL2177F and SL4177F series mitigate this issue by limiting their output to the supply rails. Refer to Figure 12 for characteristic curves illustrating this feature.

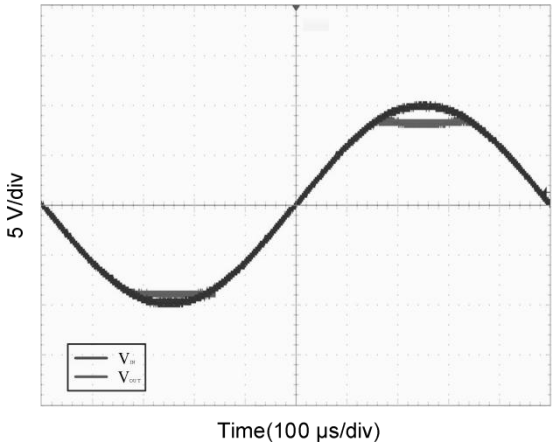


Fig.12 Phase Reversal Test Diagra

Application guide

4. Capacitive load and its stability

The SL2177F and SL4177F series can directly drive a 1nF capacitive load at unity gain without oscillation. Unity gain followers (buffers) are particularly sensitive to capacitive loads; driving a capacitive load directly can reduce the phase margin of the operational amplifier, leading to output ringing or oscillation. In applications requiring the driving of larger capacitive loads, it is advisable to add an isolation resistor R_{ISO} between the output and the capacitive load, as illustrated in Figure 13. This isolation resistor R_{ISO}, along with the capacitive load C_L, introduces a zero, thereby improving stability. A higher value of R_{ISO} enhances output stability, though at the cost of gain accuracy, as R_{ISO} and the load resistor R_L form a voltage divider network.

A more robust circuit configuration, depicted in Figure 14, offers improved stability and high DC accuracy. Connecting the inverting terminal to the output via a feedback resistor RF effectively enhances DC precision. C_F and R_{ISO} compensate for any phase margin loss. Using a high-pass element, the output signal is fed back to the inverting input, ensuring overall stability of the feedback loop.

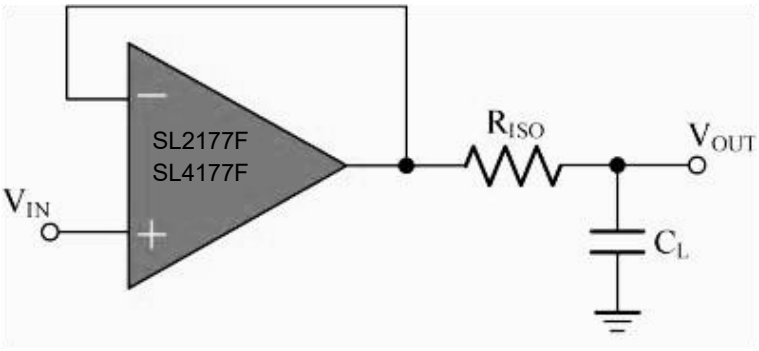


Fig.13 Indirect Driving Of Heavy Capacitive Loads

For circuits without a buffer, there are two other ways to improve the phase margin: 1) increase the gain of the op amp, or 2) add a capacitor in parallel with the feedback resistor to compensate for the parasitic capacitance at the inverting input.

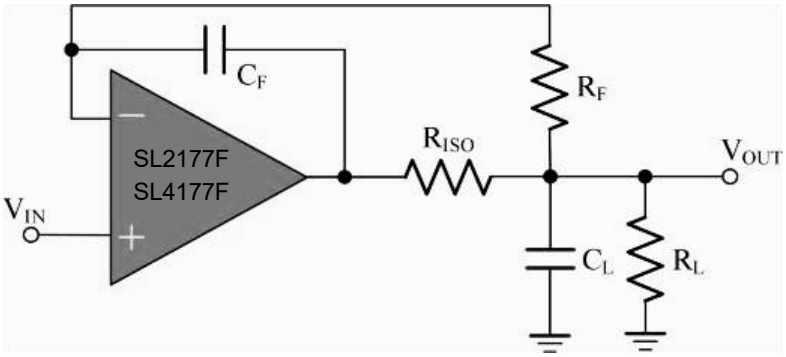


Fig.14 Directly Driving Capacitive Loads With High DC Accuracy

Application guide

5. Layout guidelines

To achieve optimal operational performance of the equipment, the following layout principles should be followed when designing a printed circuit board (PCB):

A. Divide the ground into separate digital and analog sections, carefully plan the paths for current return to ground to avoid digital signal return paths interfering with analog signals. If using a multi-layer PCB, dedicate one layer specifically to ground; this aids in heat dissipation and effectively reduces EMI noise.

B. Minimize parasitic capacitance and the proximity effect (Seebek effect) by placing external components (such as feedback resistors) as close to the chip as possible.

C. Keep input signal traces as short as possible and away from power lines or other digital signal lines.

D. Connect a low ESR, 0.1μF ceramic bypass capacitor between each power pin and ground pin, placed as close to the chip as feasible. In single-supply applications, use a capacitor to connect the chip's power pin to ground.

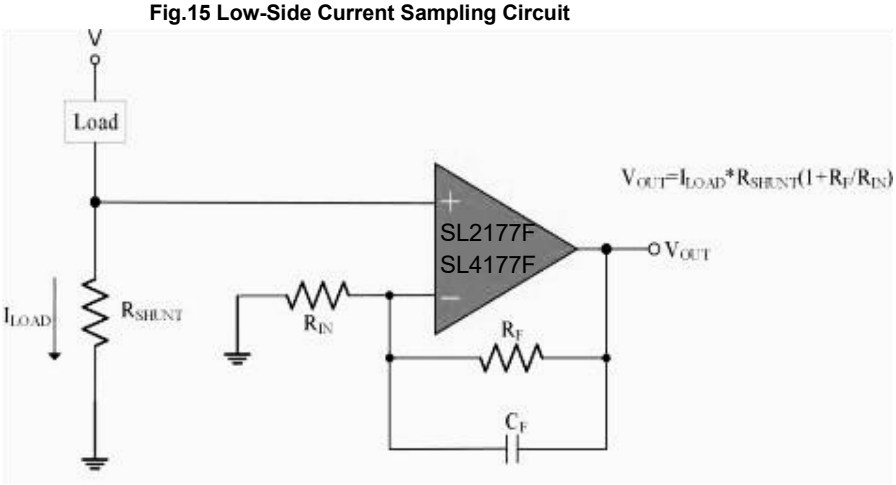
E. Consider adding a low-impedance, driven guard ring around critical wiring to significantly reduce leakage currents between different potential points.

These principles ensure efficient circuit performance and adherence to electrical engineering practices for PCB layout.

6. Low-side current sampling

As shown in Figure 15, the operational amplifier forms a low-side current sampling circuit. The load current (I_{LOAD}) generates a voltage difference across the resistor (R_{SHUNT}) and is amplified by the SL2177F and SL4177F. When the power supply voltage remains unchanged, the output voltage range can be changed by changing the resistor (R_{SHUNT}) and the closed-loop amplification factor.

Fig.15 Low-Side Current Sampling Circuit



Application guide

7. High pass filter

As shown in Figure 16, the SL2177F and SL4177F series form a bridge amplifier.

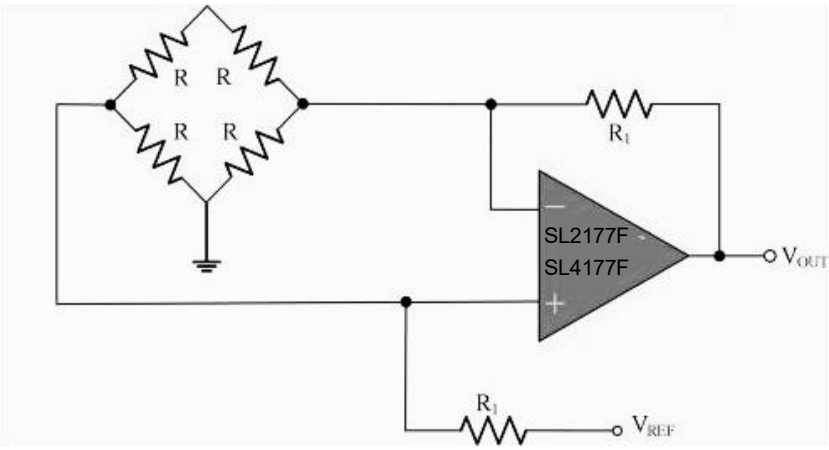


Fig.16 Bridge Amplifier

8. Programmable voltage source

As shown in Figure 17, the SL2177F and SL4177F series, along with DACs and power amplifiers, form a high-precision programmable power supply. Amplifier circuits using capacitors and resistors amplify the output voltage of the DAC, with a gain of 1+R4/R1. In applications with wide input voltage ranges, the SL2177F and SL4177F exhibit high accuracy and low drift characteristics.

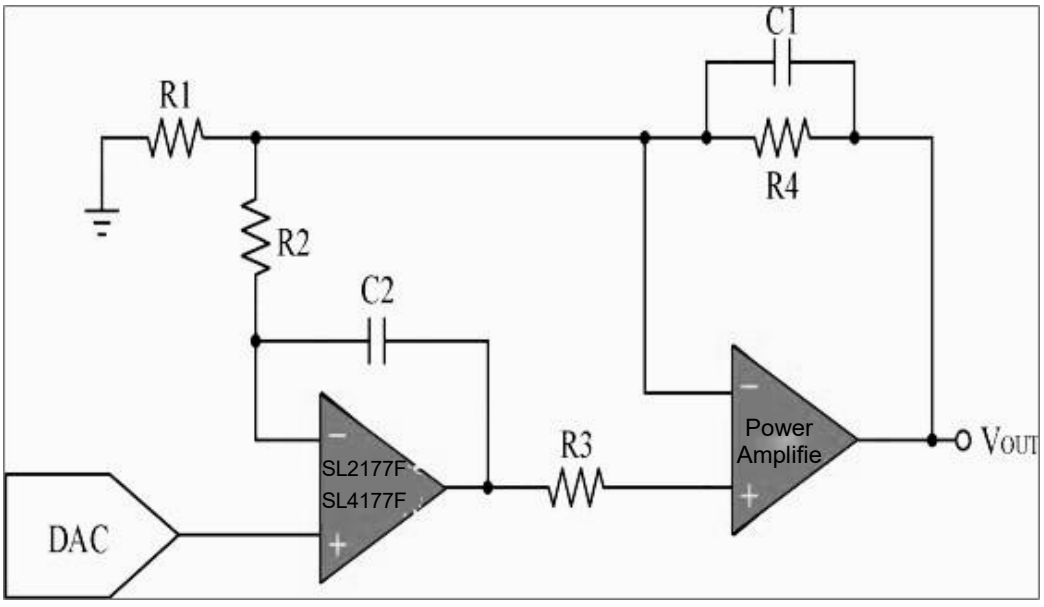
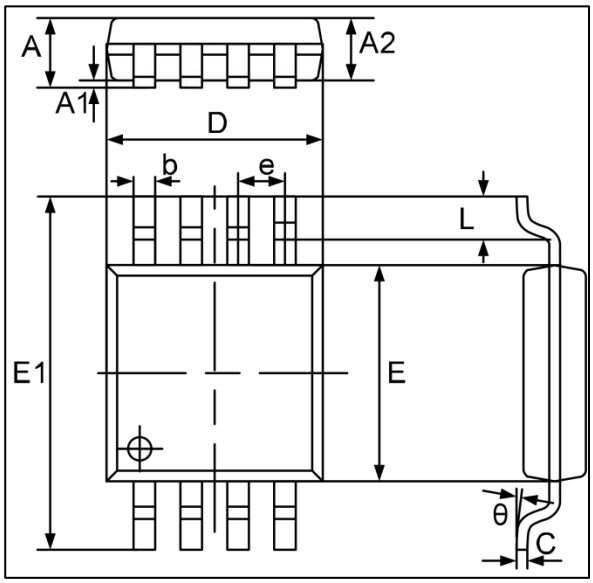


Fig.17 Programmable voltage source

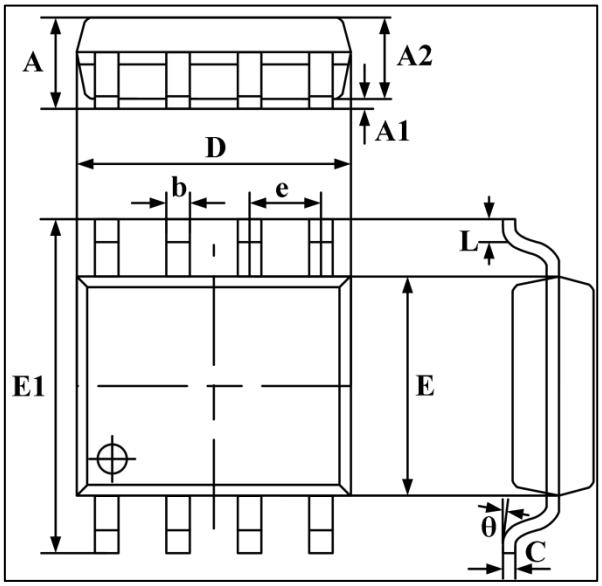
Packaging information

MSOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.033	0.045
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.031	0.039
b	0.290	0.380	0.012	0.016
C	0.150	0.200	0.006	0.008
D	2.900	3.100	0.118	0.127
E	2.900	3.100	0.118	0.127
E1	4.700	5.100	0.192	0.208
e	0.650typ.		0.026typ.	
L	0.400	0.700	0.016	0.029
θ	0°	8°	0°	8°

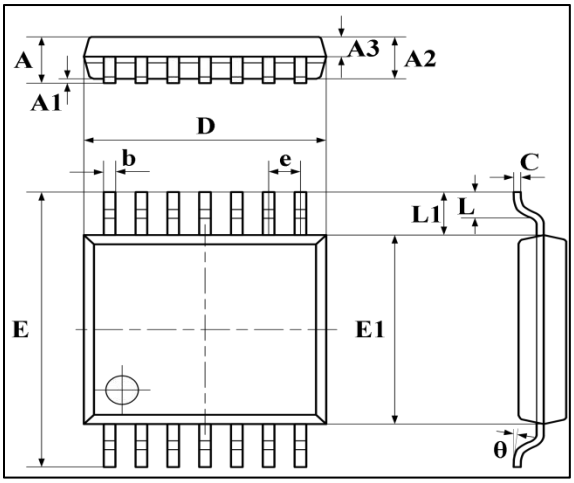
SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.370	1.670	0.056	0.068
A1	0.070	0.170	0.003	0.007
A2	1.300	1.500	0.053	0.061
b	0.306	0.506	0.013	0.021
C	0.203typ.		0.008typ.	
D	4.700	5.100	0.192	0.208
E	3.820	4.020	0.156	0.164
E1	5.800	6.200	0.237	0.253
e	1.270typ.		0.050typ.	
L	0.450	0.750	0.018	0.306
θ	0°	8°	0°	8°

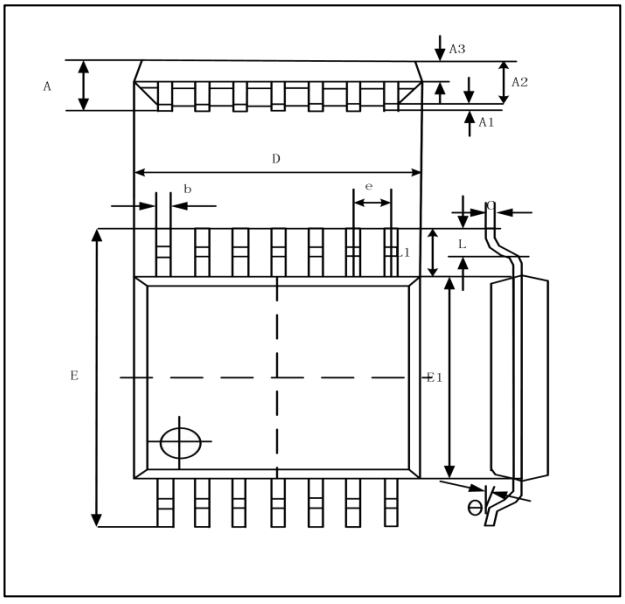
Packaging information

TSSOP-14



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	-	1.200	-	0.0472
A1	0.050	0.150	0.002	0.006
A2	0.900	1.050	0.037	0.043
A3	0.390	0.490	0.016	0.020
b	0.200	0.290	0.008	0.012
C	0.130	0.180	0.005	0.007
D	4.860	5.060	0.198	0.207
E	6.200	6.600	0.253	0.269
E1	4.300	4.500	0.176	0.184
e	0.650 typ.		0.0256 typ.	
L1	1.000 ref.		0.0393 ref.	
L	0.450	0.750	0.018	0.031
θ	0°	8°	0°	8°

SOP-14



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.450	1.850	0.059	0.076
A1	0.100	0.300	0.004	0.012
A2	1.350	1.550	0.055	0.063
A3	0.550	0.750	0.022	0.031
b	0.406typ.		0.017typ.	
C	0.203typ.		0.008typ.	
D	8.630	8.830	0.352	0.360
E	5.840	6.240	0.238	0.255
E1	3.850	4.050	0.157	0.165
e	1.270 typ.		0.050 typ.	
L1	1.040 ref.		0.041 ref.	
L	0.350	0.750	0.014	0.031
θ	2°	8°	2°	8°